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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,872	02/26/2002	Joseph A. Iadanza	BUR920010100	6213

30449 7590 01/14/2004

SCHMEISER, OLSEN + WATTS
SUITE 201
3 LEAR JET
LATHAM, NY 12033

EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

MW

Office Action Summary

Application No.	Applicant(s)
09/683,872	ladanza
Examiner	**Art Unit**
Edgardo Ortiz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 31, 2003* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above, claim(s) *17-22* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-16* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to an election filed October 31, 2003 in which Applicant elected Group I (Claims 1-16).

Election/Restriction

1. Applicant's election with traverse of Group I, claims 1-16 in Paper No. 3 is acknowledged. The traversal is on the ground that search and examination of the whole application can be done without serious burden. This is not found persuasive because, as shown in the restriction requirement mailed October 2, 2003 the inventions have a separate status in the art by their different classifications. The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-16 are rejected under 35 U.S.C. § 102 (e) as being anticipated by Bohr (U.S. Patent No. 6,617,681). With regard to Claim 1, Bohr teaches a predefined block of functional circuitry (140) having a plurality of I/O pins (118) and a backside I/O pad electrically connected to each I/O pin through a backside via (122) of an integrated circuit. See figures 4 and 6.

With regard to Claim 2, Bohr teaches I/O pins (118) formed in a lower interconnect level of an integrated circuit chip. See figures 4 and 6.

With regard to Claim 3, Bohr teaches I/O pins (118) formed in a lowest interconnect level of an integrated circuit chip. See figures 4 and 6.

With regard to Claim 4, Bohr teaches an integrated circuit that is fabricated using a bulk silicon substrate (116). See column 5, lines 65-66.

With regard to Claim 5, Bohr teaches predefined circuitry (140) that includes a first portion containing functional circuitry (142, 144) and a second portion containing I/O pins (118). See figures 4 and 6.

With regard to Claim 6, Bohr teaches a backside via (122) that connect to the I/O pins (118) in the second portion. See figures 4 and 6.

With regard to Claim 7, Bohr teaches a plurality of frontside I/O pads for the I/O pins (118) and additional I/O pins (see figure 6), each additional I/O pin electrically connected to one frontside pad of the integrated circuit by a global wiring connection. See figures 4 and 6.

With regard to Claim 8, Bohr teaches a structure that includes non-predefined circuitry (see column 6, lines 63-67 and column 7, lines 1-9).

With regard to Claim 9, Bohr teaches a plurality of frontside I/O pads for the I/O pins (118) and the non-predefined circuitry having a plurality of I/O pins (see column 6, lines 63-67 and column 7, lines 1-9), each additional I/O pin of the non-predefined circuitry electrically connected to one frontside I/O pad of the integrated circuit by a global wiring connection. See figures 4 and 6.

With regard to Claim 10, Bohr teaches additional predefined circuit I/O pins (see column 6, lines 63-67 and column 7, lines 1-9), each additional predefined circuit I/O pin of the non-predefined circuitry electrically connected to one frontside I/O pad of the integrated circuit by a global wiring connection.

With regard to Claim 11, Bohr teaches providing a predefined block of functional circuitry (140) having a plurality of I/O pins (118) and connecting a backside I/O pad electrically connected to each I/O pin through a backside via (122) of an integrated circuit. See figures 4 and 6.

With regard to Claim 12, Bohr teaches providing additional I/O pins and electrically connecting each additional I/O pin to one frontside I/O pad of the integrated circuit by a global wiring connection. See figures 4 and 6.

With regard to Claim 13, Bohr teaches providing non-predefined circuitry (see column 6, lines 63-67 and column 7, lines 1-9).

With regard to Claim 14, Bohr teaches providing a plurality of frontside I/O pads for the I/O pins (118) and electrically connecting each additional I/O pin to one frontside I/O pad of the integrated circuit by a global wiring connection. See figures 4 and 6.

With regard to Claim 15, Bohr teaches providing additional predefined circuit I/O pins (see column 6, lines 63-67 and column 7, lines 1-9), and electrically connecting each additional I/O pin to one I/O frontside pad of the integrated circuit by a global wiring connection.

With regard to Claim 16, Bohr teaches forming a backside via (122) in a bulk silicon substrate (116). See column 5, lines 65-66 and see figures 4 and 6.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached through a direct telephone call, you might call Supervisor Tom Thomas at (703) 308-2772. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

ALLAN R. WILSON
PRIMARY EXAMINER

1/8/04